a semiconductor substrate including first and second laterally-extending layers of first and second opposite polarity dopants defining a body layer and an underlying drain layer;

a first trench having sidewalls extending depthwise from an upper surface of the substrate at least through the body layer to a bottom wall at a first predetermined depth from the upper surface of the substrate;

a gate oxide layer on the first trench sidewalls and bottom wall;

a gate conductor filling the first trench depthwise to at least an elevation of the upper surface of the substrate and contacting the gate oxide layer on the trench sidewalls;

a second trench having sidewalls extending depthwise from the upper surface of the substrate to a bottom wall at a second predetermined depth in the body layer spaced above the drain layer, the first trench and the second trench being spaced apart by a predetermined lateral distance;

a vertically oriented layer of the semiconductor substrate laterally positioned between the first trench and the second trench and extending upward along the gate oxide layer from the body layer to the upper surface of the substrate; and

a vertically-extending source conductor contacting the bottom wall and sidewalls of the second trench including contacting the vertically oriented [layers on both sides] layer on a side of the second trench and opposite the gate oxide layer and gate conductor and contacting the laterally-extending body layer along the bottom wall;

the vertically-oriented layer including a first vertical layer portion contiguous with the body layer doped with said first polarity dopant and a second vertical layer portion atop the first vertical layer portion and doped with [a] said second polarity dopant to form a PN junction with the first vertical layer portion;

the first vertical layer portion being doped with said first polarity dopant to a first doping concentration to define an active body region, including a vertical channel having a

threshold characteristic determined by the first doping concentration;

the second vertical layer portion being doped with said second polarity dopant to form a source region contacting the active body region;

the source conductor electrically shorting the source region to the active body region across the PN junction; and

a top portion of the body layer extending horizontally and confined to the bottom of the second trench, spaced depthwise along the trench sidewalls below the PN [junctions] junction, in contact with the source conductor along the bottom wall, being doped to a second doping concentration contained within the body layer, the second doping concentration being greater than the first doping concentration and sufficient to reduce pinched base resistance and thereby prevent parasitic bipolar turnon in the presence of avalanche current, independent of the threshold characteristic of the vertical channel in the active body region[.]; the vertically-oriented layer having a lateral thickness of less than 0.5 micron.

36. (First amendment) A recessed gate field effect power MOS device according to claim 35 including [one of said vertically-oriented layers] on each side of the second trench, each side having one [of] said vertically-oriented insulative [layers] layer thereon, and an insulative layer extending laterally between the [sidewall spacers] vertically-oriented insulative layers over the gate conductor.

39. (First amendment) A recessed gate field effect power MOS device according to claim [34] 40 in which the vertically-oriented layer has a lateral thickness of less than 0.5 micron.

Add new claims 40-42 as follows:

--40. A recessed gate field effect power MOS device having a vertically oriented channel comprising:

a semiconductor substrate including first and second laterally-extending layers of first

and second opposite polarity dopants defining a body layer and an underlying drain layer;

a first trench having sidewalls extending depthwise from an upper surface of the substrate at least through the body layer to a bottom wall at a first predetermined depth from the upper surface of the substrate;

a gate oxide layer on the first trench sidewalls and bottom wall;

a gate conductor filling the first trench depthwise to at least an elevation of the upper surface of the substrate and contacting the gate oxide layer on the trench sidewalls;

a second trench having sidewalls extending depthwise from the upper surface of the substrate to a bottom wall at a second predetermined depth in the body layer spaced above the drain layer, the first trench and the second trench being spaced apart by a predetermined lateral distance;

a vertically oriented layer of the semiconductor substrate laterally positioned between the first trench and the second trench and extending upward along the gate oxide layer from the body layer to the upper surface of the substrate; and

a vertically-extending source conductor contacting the bottom wall and sidewalls of the second trench including contacting the vertically oriented layer on a side of the second trench and opposite the gate oxide layer and gate conductor and contacting the laterally-extending body layer along the bottom wall;

the vertically-oriented layer including a first vertical layer portion contiguous with the body layer doped with said first polarity dopant and a second vertical layer portion atop the first vertical layer portion and doped with said second polarity dopant to form a PN junction with the first vertical layer portion;

vertically-oriented insulative layers on opposite sides of the first trench and gate conductor, aligned above the vertically-oriented layer of the semiconductor substrate and the gate oxide layer; and

an insulative layer extending laterally between the vertically-oriented insulative layers over the gate conductor;

the vertically-insulative layers being formed by a deposited film of uniform lateral thickness and the laterally-extending insulative layer being separately formed of a deposited isolation material.--

fig. 20, 21 C5 Cont

--41. A recessed gate field effect power MOS device according to claim 40 in which the vertically oriented layer and the gate oxide layer have a combined lateral thickness less than a lateral thickness of the vertically-oriented insulative layer.--

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--42. A recessed gate field effect power MOS device according to claim 40 in which the lateral thickness of the vertically-oriented insulative layer is in a range of 0.5 to 1.0 micrometer.--

REMARKS

Pending Claims 23; 30-39 stand rejected under 35 U.S.C. 112. Claims 23, 31, 32, 34-36 and 39 under 35 U.S.C. 103(a) stand rejected as obvious from Sakamoto in view of Davies and claims 30 and 33 further in view of Blanchard; and claims 37 and 38 over Sakamoto in view of Blanchard and Wickstrom.

Claims 31, 34, and 36 are amended to remove the § 112 objections. New independent claim 40 is added based on claims 34 and 36 to claim distinguishing features of the spacer (vertically-oriented insulative layer) in applicant's invention.

New claims 41 and 42 depend the subject matter of claims 37 and 38 from claim 40.

Claims 23, 30-39 and 40-42 remain in the case.

Response to §112 Rejections

Applicant traverses the rejection of claim 38 under § 112(1). The Examiner states that the lateral thickness of the sidewall spacer as disclosed on page 16, lines 19-21 is 0.8 to 1.0